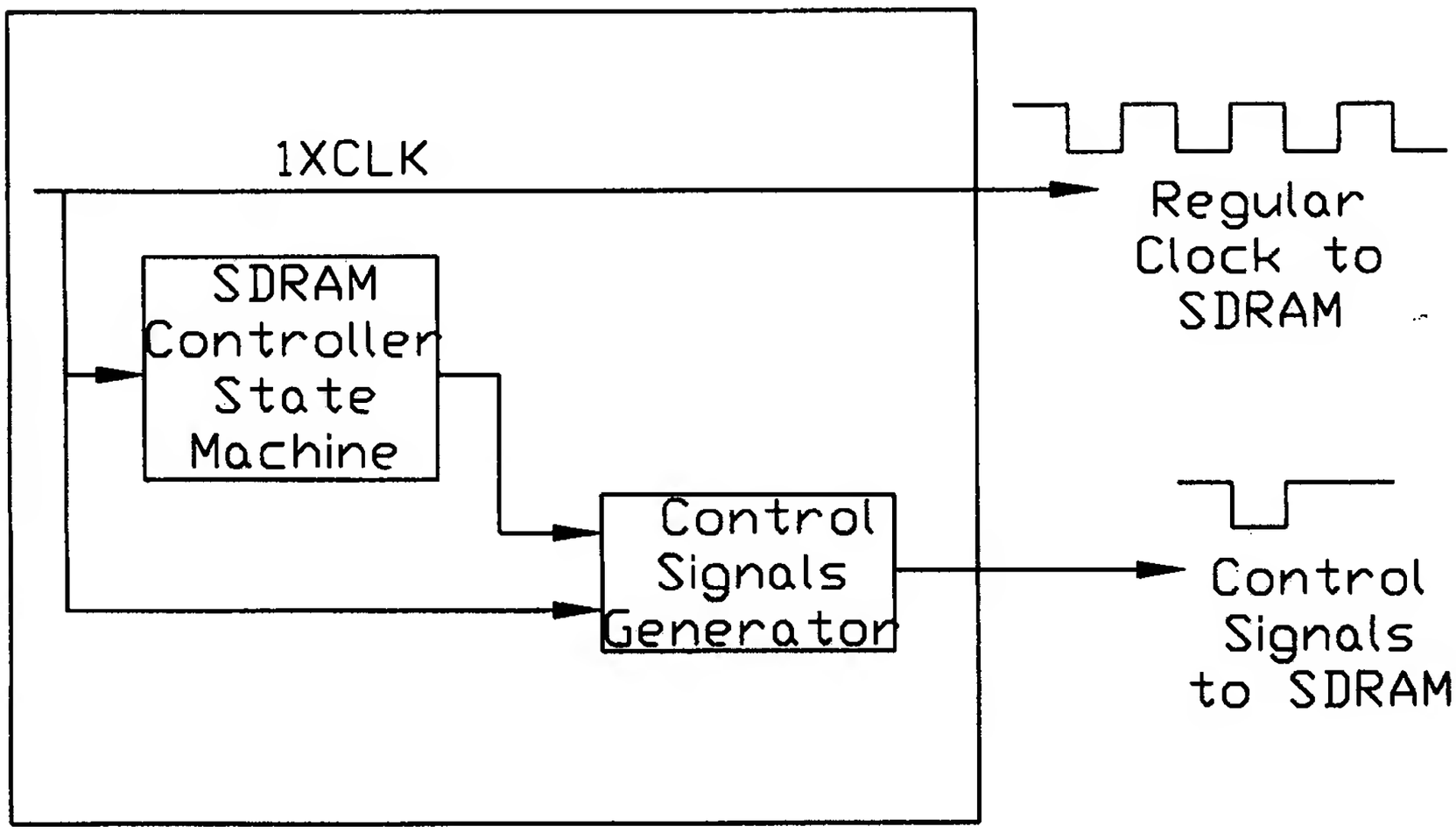
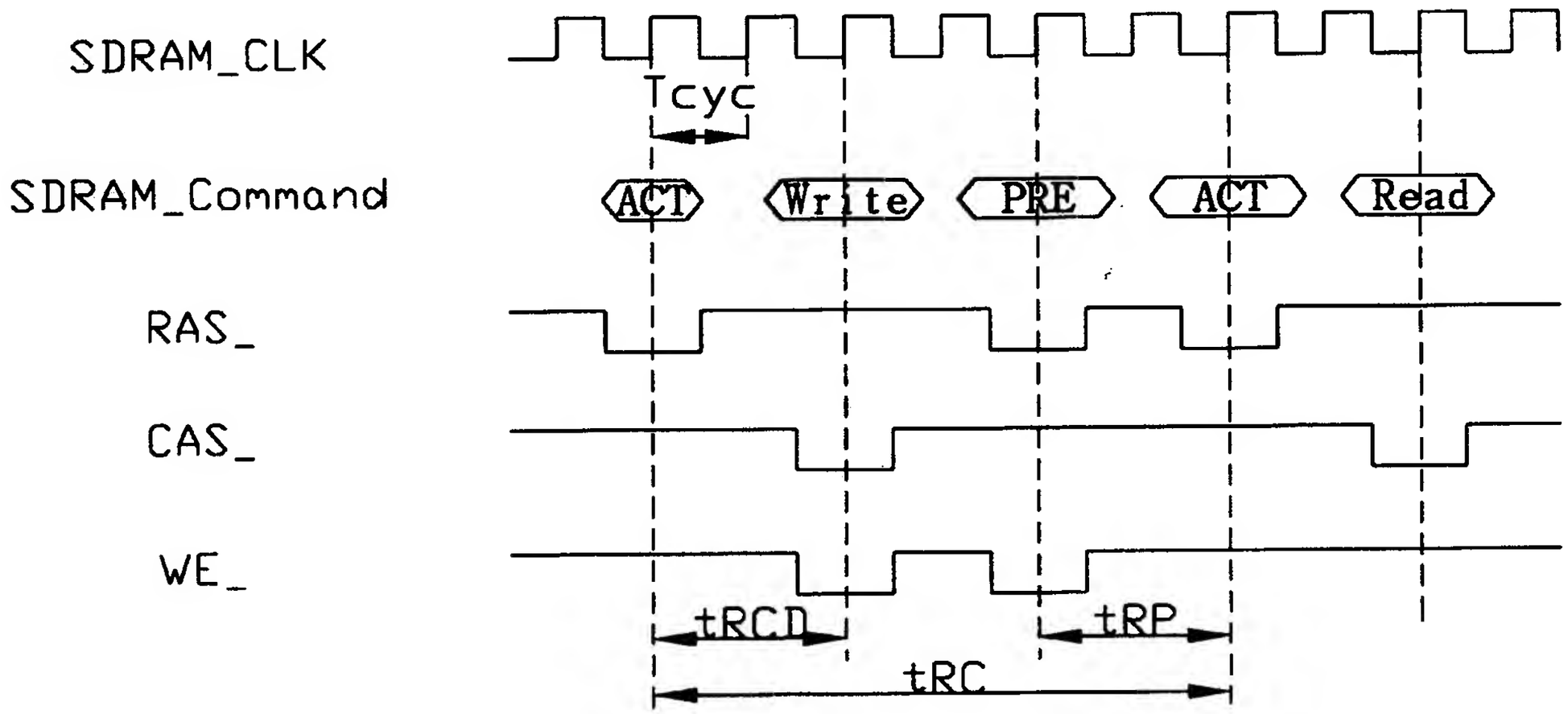


FIG.1(Prior Art)



ACT:Active Command
Write: Write Command
Read: Read Command
PRE: Pre-Charge Command

tRCD: RAS_to CAS_delay time
tRCDmin: minimum time for tRCD
tRP: RAS pre-charge time
tRPmin: minimum time for Trp
tRC: Command Period
tRCmin: minimum time for tRC

tRCD=2*Tcyc
tRCDmin=1.4*Tcyc
tRP=2*Tcyc
tRPmin=1.4*Tcyc
tRC=6*Tcyc
tRCmin=5*Tcyc

FIG.2(Prior Art)

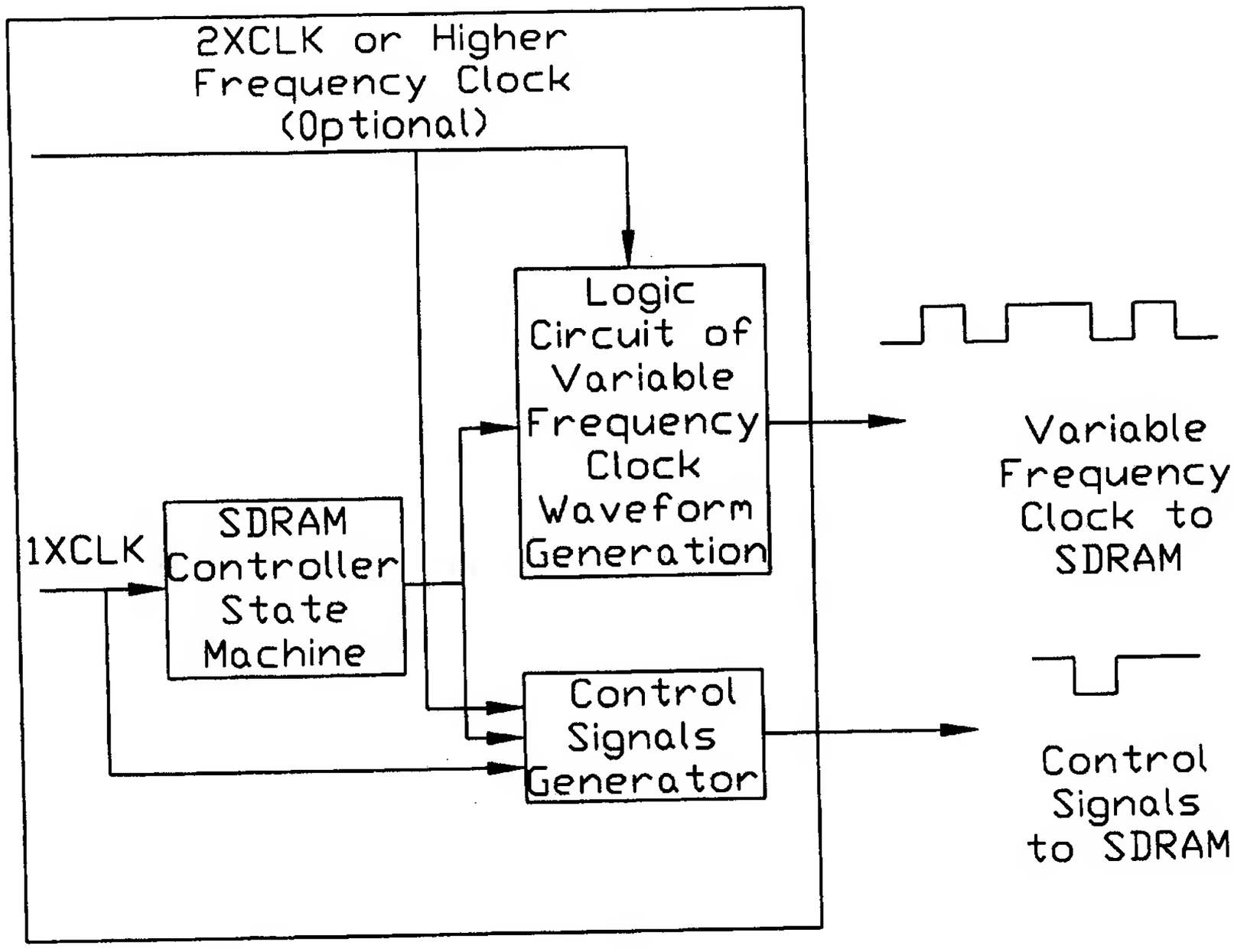
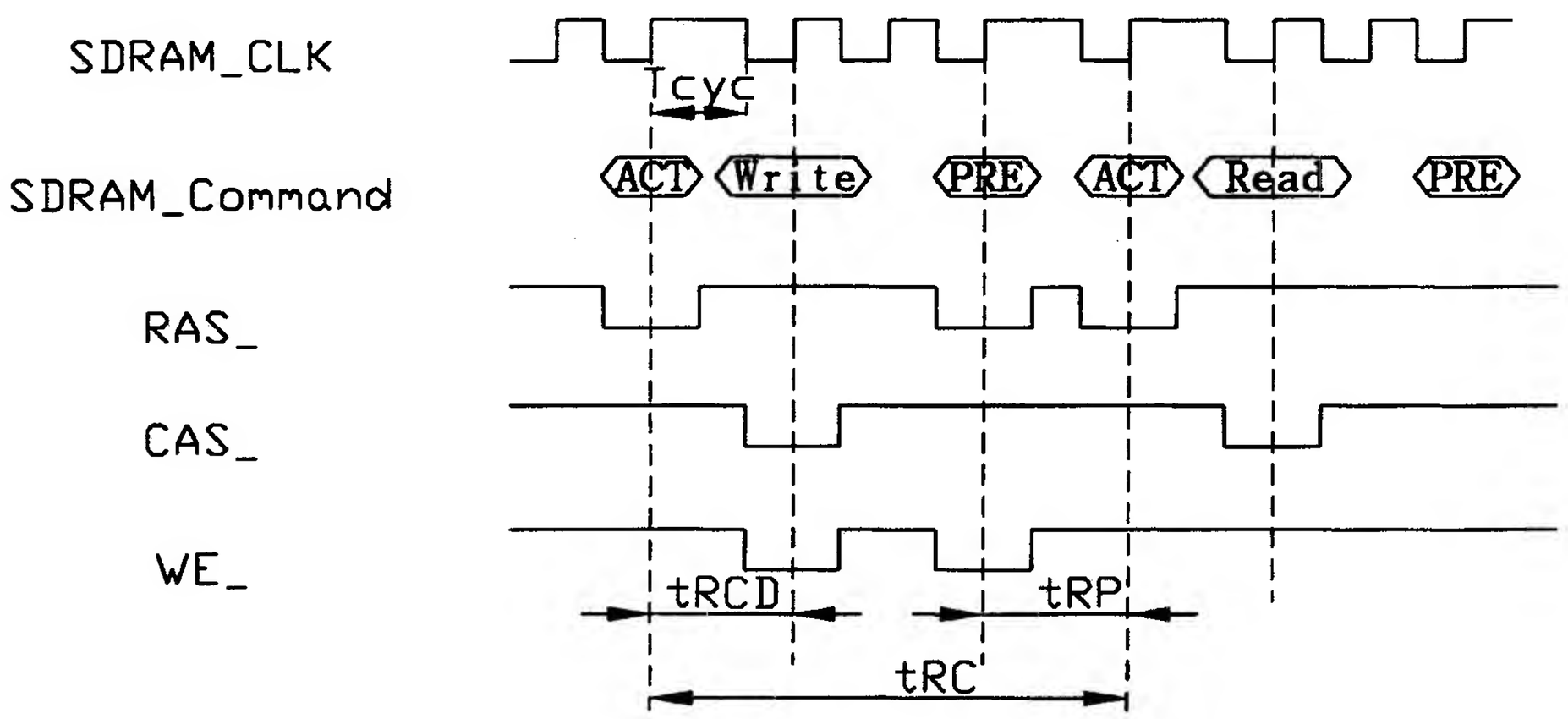

2XCLK or Higher
Frequency Clock
(Optional)
Logic
Circuit of
Variable
Frequency
Clock
Waveform
Generation
Variable
Frequency
Clock to
SDRAM
1XCLK
SDRAM
Controller
State
Machine
Control
Signals
Generator
Control
Signals
to SDRAM

FIG.3



ACT:Active Command
Write: Write Command
Read: Read Command
PRE: Pre-Charge Command

tRCD: RAS_to CAS_delay time
tRCDmin: minimum time for tRCD
tRP: RAS pre-charge time
tRPmin: minimum time for Trp
tRC: Command Period
tRCmin: minimum time for tRC

tRCD=2*Tcyc
tRCDmin=1.4*Tcyc
tRP=2*Tcyc
tRPmin=1.4*Tcyc
tRC=6*Tcyc
tRCmin=5*Tcyc

FIG.4